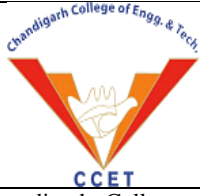


Tender No. CCET/DG/SPA/2019/04

Dated:- 18.12.2019



CHANDIGARH COLLEGE OF ENGINEERING & TECHNOLOGY (DEGREE WING), SECTOR 26, CHANDIGARH
(FAX No. 0172-2750872, Phone No. 0172-2750943)
E-TENDER NOTICE
College website: - www.ccet.ac.in

Chandigarh College of Engineering & Technology (Degree Wing), Sector-26, Chandigarh invites e-tenders for the **purchase of equipments in the Labs of Electronics and Communication Engineering Department** on item-wise basis for each scheme. The dates for opening and closing of e-tender are as given below:-

Start Date and Time of uploading of e-tender	End Date and Time of uploading of e-tender	Date and Time of opening of Online Bid (Technical Bid)	Earnest Money
19.12.2019 at 9.00 AM	09.01.2020 at 11.00 AM	09.01.2020 at 11.30 AM	Detail of Earnest Money to be deposited is available in the e-tender document.

Detailed Terms and Conditions including detail of Earnest Money are available in e-tender document.

The bid document can be downloaded from the website of Chandigarh Administration <https://etenders.chd.nic.in> however for general information, guidance and reference; the tenderer can approach to office of Principal, Chandigarh College of Engineering & Technology, (Degree Wing), Sector-26, Chandigarh (Phone No. 0172-2750943)

Principal



**CHANDIGARH COLLEGE OF ENGINEERING & TECHNOLOGY,(DEGREE WING),
SECTOR 26, CHANDIGARH
(Phone No. 0172-2750943)
E-TENDER NOTICE
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Chandigarh College of Engineering & Technology (Degree Wing), Sector-26, Chandigarh invites tenders through e-tendering the purchase of equipments in the Labs of Electronics and Communication Engineering Department on item-wise basis for each scheme :-

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT				
Scheme Name	Item No.	Item	Quantity	Earnest Money (In Rs.)
SCHEME –I ADVANCE DIGITAL COMMUNICATION LAB	1.	<p>DSB/SSB AM Transmitter</p> <p>Features A self contained Trainer Functional blocks indicated on board mimic Input-output and Test Points provided onboard Built in DC Power Supply Fully documented student work book & operating manual 8 Switched faults Crystal controlled carrier frequency On-board audio, modulator, carrier frequency generation, antenna & speaker</p> <p>Technical Specification Audio Oscillator : With adjustable Amplitude & Frequency (300 Hz - 3.4 KHz) Audio Output : Amplifier with speaker Modulators : Balanced Modulator with Band pass Filter (1 MHz) - 2 Nos. Balanced Modulator (455 KHz) - 1 No. Ceramic Bandpass Filter - 1 No. Carrier Frequency : 1 MHz (Crystal controlled) Transmitter Amplifier Output : (Gain adjustable) DSB (1 MHz), SSB (1.445 MHz) connected to Antenna/cable Switched Faults : 8 nos. Interconnections : 4mm Banana Socket Test Points : 27 nos (Gold plated) Power Supply : 230 V \pm10%, 50/60 Hz Power Consumption : 4 VA approximately Operating Conditions : 0-40 C, 80% RH Included Accessories : Patch Cord 16" : 2 nos. Mains Cord : 1 no. Microphone : 1 no. Learning Material (CD) : 1 no. CD (Demo VCD) providing : 1 no. ACT book providing with full set only: 1 no. Learning Software for Analog Communication.</p> <p>Experiment Performed Study of carrier frequency generation. Study of DSB & SSB AM generation & Transmission. Study of Transmitter tuned circuits. Study of Modulation index.</p>	02	2260.00
	2.	<p>DSB/SSB AM Receiver</p> <p>Features A self contained Trainer Functional blocks indicated on board mimic Input-output and Test Points provided onboard Built in DC Power Supply Exhaustive learning material 8 Switched Faults Effect of AGC on the detection of DSB AM signal may be Investigated On board RF Amplifier, Mixer, IF amplifier, Diode detector, Product detector, Audio amplifier.</p> <p>Technical Specification Construction : Superhetrodyne Frequency Range : 980 KHz to 2060 KHz Intermediate Frequency : 455 KHz Input Circuits : 1) RF Amplifier</p>	02	2460.00

	<p>2) Mixer 3) Local Oscillator 4) Beat Frequency Oscillator 5) IF Amplifier 1 6) IF Amplifier 2 Tuning : With Variable Capacitor (ganged) Dial marking on Board Receiving media : Telescopic Antenna / Cable Detectors: 1) Diode Detector (For DSB) 2) Product Detector (SSB) Audio Output : Amplifier with Speaker Automatic Gain control : Switchable Switched Faults : 8 nos. Interconnections : 2 mm Banana Sockets Test points : 50 nos (Gold plated) Power Supply : 230 V \pm10 %, 50/60 Hz Power Consumption : 3 VA approximately Operating Conditions : 0-40 C, 80% RH Included Accessories : Patch cord 16" : 2 nos. Mains cord : 1 no. Microphone : 1 no. Learning Software for Analog Communication. <u>Experiment Performed</u> Study of DSB & SSB AM reception & detection by diode / product detectors Study of AGC Study of Receiver tuned circuits Study of Sensitivity, Selectivity & Fidelity of Receiver</p>		
3.	<p>Frequency Modulation & Demodulation <u>Features</u> A self contained platform Functional blocks indicated on board mimic Input – Output and Test points provided onboard Built-in DC Power Supply Exhaustive learning material 8 switched faults On board audio, modulators, detectors, amplitude limiter & filter circuits Effect of noise on the detection of FM signal may be investigated <u>Technical Specification</u> Audio Oscillator : With adjustable Amplitude & Frequency (300 Hz – 3.4 KHz) Audio Oscillator : With adjustable Amplitude & Frequency (300 Hz – 3.4 KHz) FM Modulator : 2 nos. 1) Reactance Modulator (with carrier Frequency adjustment) 2) Varactor Modulator (with carrier Frequency adjustment) Mixer / Amplifier : 1 no. (With Gain adjustment) Allows FM input signal to be amplitude modulated by a noise input prior to demodulation. Transmitter Output : 455 KHz Frequency FM Demodulator : 5 nos. 1) Detuned Resonant Detector 2) Quadrature Detector 3) Foster – Seeley Detector 4) Ratio – Detector 5) Phase Locked Loop Detector Low Pass Filter : 3.4 KHz Cut off Frequency Amplifier (with adjustable gain) Amplitude Limiter : 1 no. Switched Faults : 8 nos. Interconnections : 4 mm banana sockets Test points : 74 nos (Gold plated) Power Supply : 230 V \pm10%, 50 / 60 Hz Power Consumption : 3 VA approximately Operating Conditions : 0-40 C, 80% RH Included Accessories : Patch cord 16" : 4 nos. Mains cord : 1 no. Learning Software for Analog Communication. <u>Experiment Performed</u> Study of Frequency Modulation using Varactor</p>	02	2260.00

	<p>modulator</p> <p>Study of Frequency Modulation Using Reactance Modulator</p> <p>Study of Operation of Detuned Resonant Circuit</p> <p>Study of Operation of Quadrature Detector</p> <p>Study of Operation of Phase-Locked Loop Detector</p> <p>Study of Operation of Foster – Seeley Detector</p> <p>Study of Operation of Ratio Detector</p>		
4.	<p>Digital Companding A-law and u-law</p> <p><u>Features & Technical Specification</u></p> <p>Compression and Decompression of data on same board</p> <p>On-board DDS Signal Generator</p> <p>Compression and Decompression</p> <p>Techniques : A-Law</p> <p style="padding-left: 40px;">μ-Law</p> <p>Signal Generator : Generated Sine wave</p> <p>14 Bit data input through Dip switch.</p> <p>SMD LED Indicators : 73nos, for</p> <p>Dip based input data</p> <p>Compressed output</p> <p>Decompressed output</p> <p>Technique selection</p> <p>Crystal Frequency : 8MHz</p> <p>Test Points : 37nos (Gold plated).</p> <p>Direct Digital Synthesizer</p> <p>Power Supply : 110V – 260V AC, 50/60Hz</p> <p>Operating Conditions : 0-40 C, 85% RH</p> <p>Included accessories : 2mm Patch cord – 2nos, FRC Cable 16 pins -1no</p> <p><u>Experiment Performed</u></p> <p>Study and analysis of A-law Compression.</p> <p>Study and analysis of μ-law Compression.</p> <p>Study and analysis of A-law Decompression.</p> <p>Study and analysis of μ-law Decompression</p>	02	3540.00
5.	<p>Error Detection and Correction of Cycle Codes</p> <p><u>Features & Technical Specification</u></p> <p>On-board data and code clock generation</p> <p>On-board data generator</p> <p>BCD rotary switches for data selection</p> <p>LED numeric display</p> <p>Multiple data rate and code rate selection</p> <p>Seven bit code for four bit running or static data</p> <p>Single bit error detection and correction</p> <p>Crystal Frequency : 4.096 MHz</p> <p>Data Rates : 16 KHz, 8 KHz, 4 KHz, 2 KHz and 1 KHz</p> <p>Code Rates : 32 KHz, 16 KHz, 8 KHz, 4 KHz and 2 KHz</p> <p>Word Length : 4 bits</p> <p>Code Length : 7 bits code and 1 stuffed bit</p> <p>Data Format : NRZ (Not Return to Zero)</p> <p>Test Points : 45 nos (Gold plated)</p> <p>Interconnections : 2 mm Sockets (Gold plated)</p> <p>Internal Operating Voltage : + 5V DC</p> <p>Power Supply : 110V – 260V AC, 50/60Hz</p> <p>Operating Conditions : 0-40 C, 85% RH</p> <p>Included Accessories :</p> <p>Patch cord 8" : 20 nos</p> <p>Power Supply : 1 no.</p> <p>Learning Material (CD) : 1 no.</p> <p><u>Experiment Performed</u></p> <p>Study of Cyclic Encoding and Decoding of BCD bit sequence</p> <p>Study of Error Detection & Correction of bits sequence</p>	02	3380.00
6.	<p>Understanding Block Code Encoder</p> <p><u>Features & Technical Specification</u></p> <p>On-board clock generation for Data and Code.</p> <p>On-board data generator.</p> <p>On board error generator block</p> <p>BCD rotary switches for Data Selection.</p> <p>LED Numeric display.</p> <p>Single bit error detection and correction.</p> <p>Default and manual H-matrix selection</p> <p>Exhaustive learning material</p>	02	3740.00

	<p>Crystal Frequency : 11.059 MHz Word Length : 4 bits Codeword Length : 7 bits code Data Format : NRZ (Not Return to Zero) Interconnections : 2 mm sockets (Gold plated) Test points : 5 nos (Gold plated) Power Supply : 110-220 V \pm10%, 50/60 Hz Operating Conditions : 0-40 C, 80% RH Internal Power supply : +5V DC Included Accessories : Patch cord 8" : 12 nos. Power supply : 2 nos. Mains cord : 2 nos.</p> <p><u>Experiment Performed</u> Study of Hamming Code (7,4)-bit Generation Study of Hamming Code (Encoding & Decoding) without bit error Study of Hamming Code (Encoding and Decoding) of BCD bit sequence in manual mode. Study of Hamming Code (7,4)-bit Generation Without error With single bit error With double bit error</p>		
7.	<p>Understanding Block Code Decoder <u>Features & Technical Specification</u> On-board clock generation for Data and Code. On-board data generator. On board error generator block BCD rotary switches for Data Selection. LED Numeric display. Single bit error detection and correction. Default and manual H-matrix selection Exhaustive learning material Crystal Frequency : 11.059 MHz Word Length : 4 bits Codeword Length : 7 bits code Data Format : NRZ (Not Return to Zero) Interconnections : 2 mm sockets (Gold plated) Test points : 5 nos (Gold plated) Power Supply : 110-220 V \pm10%, 50/60 Hz Operating Conditions : 0-40 C, 80% RH Internal Power supply : +5V DC Included Accessories : Patch cord 8" : 12 nos. Power supply : 2 nos. Mains cord : 2 nos.</p> <p><u>Experiment Performed</u> Study of Hamming Code (7,4)-bit Generation Study of Hamming Code (Encoding & Decoding) without bit error Study of Hamming Code (Encoding and Decoding) of BCD bit sequence in manual mode. Study of Hamming Code (7,4)-bit Generation Without error With single bit error With double bit error</p>	02	3740.00
8.	<p>Training system for study of PAM, PWM and PPM <u>Technical Specification</u> Training system for understanding the Pulse Amplitude Modulation and Demodulation, Pulse Width Modulation and Demodulation and Pulse Position Modulation and Demodulation. On board provision should be for generation of data pattern up to 8, 16 and 32 bit and signal generation (Sine, Square & Arbitrary) with variable frequency along with variable sampling frequency. Also this training system should be of study for different types of line coding i.e. of NRZ Unipolar Coding, NRZ Polar Coding, NRZ Bipolar Coding, RZ Polar Coding, Manchester Coding and analyze all types of Line Coding outputs simultaneously and Observe differences. Specifications: Modulation Technique : Pulse Amplitude Modulation and Demodulation</p>	01	1770.00

	<p>Pulse Width Modulation and Demodulation Pulse Position Modulation and Demodulation Line Coding Techniques Crystal Frequency: 20MHz DDS Signal Generator: Sine, Square, Triangle, arbitrary signal Input Signal Frequency: 305Hz, 609.80Hz, 1.25KHz, 2.5KHz Sampling Frequency: 1.25KHz, 2.50KHz, 5KHz, 9.80KHz, 19.53KHz, 39.06KHz, 78.13KHz Ramp Frequency: 1.25KHz, 2.50KHz, 5KHz, 9.80KHz, 19.53KHz, 39.06KHz, 78.13KHz</p> <p>Low Pass Filter: Cut-off frequency 5KHz Should be gold plated for good ohmic contact & More than 30 nos. for waveform observation.</p>		
9.	<p>Training system for study of PCM, DPCM, CVSD Modulation & Demodulation Technical Specification Training system for understanding the Pulse Code Modulation and Demodulation, Differential Pulse Code Modulation and Demodulation and Continuously Variable Slope Delta Modulation and Demodulation. On board provision should be for generation of DDS signal generation (Sine, Square, Triangle & Arbitrary) with variable frequency along with variable sampling frequency. Also this training system should be of study for effect of channel (channel as a attenuator, as a low pass, as a noise) between transmitter and receiver and analyze its effects Specifications: Modulation Technique : Pulse Code Modulation and Demodulation. Differential Pulse Code Modulation and Demodulation Continuously Variable Slope Delta Modulation and Demodulation Crystal Frequency : 8MHz DDS Signal Generator : Sine, Square, Triangle, arbitrary signal Input Signal Frequency: 500Hz,1KHz,1.5KHz,2KHz,3KHz Sampling Frequency: 4KHz, 8KHz, 16KHz, 32KHz Line Speed: 32KHz, 64KHz, 128KHz, 256KHz Noise Gain: Variable Low Pass Filter: Cut-off frequency 5KHz Should be gold plated for good ohmic contact & More than 30 nos. for waveform observation Channel Effect : Channel as a low-pass Channel as a attenuator Channel as a noise</p>	01	1900.00
10.	<p>Training system for study of Delta, Adaptive Delta & Sigma Delta Modulation & Demodulation Technical Specification Training system for understanding the of Delta , Adaptive Delta & Sigma Delta Modulation & Demodulation. On board provision should be for generation of DDS signal generation (Sine, Square, Triangle & Arbitrary) with variable frequency along with variable sampling frequency. Also this training system should be of study for effect of channel (channel as a attenuator, as a low pass, as a noise) between transmitter and receiver and analyze its effects Specifications: Modulation Technique : Delta Modulation and Demodulation. Adaptive Delta Modulation and Demodulation Delta Sigma First Order Modulation and Demodulation Delta Sigma Second Order Modulation and Demodulation Crystal Frequency: 8MHz DDS Signal Generator: Sine, Square, Triangle, arbitrary signal Input Signal Frequency: 500Hz, 1KHz, 1.5KHz, 2KHz, 3KHz</p>	01	1980.00

	<p>Sampling Frequency: 16KHz, 32KHz, 64KHz, 128KHz , 256KHz Noise Gain: Variable Integrator(step size): 1,3,5</p> <p>Low Pass Filter: Cut-off frequency 5KHz Test Points: Should be gold plated for good ohmic contact & More than 40 nos. for waveform observation Channel Effect : Channel as a low-pass Channel as a attenuator Channel as a noise</p>		
11.	<p>Training System for study of ASK, FSK, BPSK, DBPSK Modulation & Demodulation</p> <p>Technical Specification Training system for understanding the of ASK, FSK, BPSK,DBPSK Modulation & Demodulation. On board provision should be for internal data generation up to 64 bits with variable frequency .</p> <p>Specifications: Modulation & Demodulation Techniques: ASK, FSK, BPSK and DBPSK Internal Data Generator : Digital Data Data Pattern : 8-Bit , 16-Bit , 32-Bit , 64-Bit Frequency : 2KHz, 4KHz, 8KHz, 16KHz Internal Carrier Generator : Direct Digital Synthesized Carrier Signal : Sine, Cosine SMD LED Indicators : For Digital Data Selection, Data frequency selection, Technique selection Test Points: Should be gold plated for good ohmic contact & More than 40 nos. for waveform observation Crystal Frequency : 8MHz Selection Mode : Push switches</p>	01	1930.00
12.	<p>Training System for study of QPSK, OQPSK, DQPSK Modulation & Demodulation</p> <p>Training system for understanding the of QPSK, OQPSK, DQPSK Modulation & Demodulation. On board provision should be for internal data generation up to 64 bits with variable frequency.</p> <p>Specifications: Modulation & Demodulation Techniques: QPSK, OQPSK and DQPSK Internal Data Generator : Digital Data Data Pattern : 8-Bit , 16-Bit , 32-Bit , 64-Bit Frequency : 2KHz, 4KHz, 8KHz, 16KHz Internal Carrier Generator : Direct Digital Synthesized Carrier Signal : Sine, Cosine SMD LED Indicators : For Digital Data Selection, Data frequency selection, Technique selection Test Points: Should be gold plated for good ohmic contact & More than 50 nos. for waveform observation Crystal Frequency : 8MHz Selection Mode : Push switches</p>	01	1930.00
13.	<p>Training System for study of MSK, GMSK, FSK, GFSK, Modulation & Demodulation</p> <p>Training system for understanding the of MSK, GMSK, FSK, GFSK Modulator and Demodulator with AWGN Channel Noise. On board provision should be for internal data generation up to 64 bits with variable frequency with reconfigurable modulation index and data rate. It should have built in hardware for time domain signal analysis. Training system should have provision for understanding of BER measurement using actual bit errors with a known digital data test sequence at the transmitter end. It should have of Interface USB and Matlab interface utility</p> <p>Specifications: Modulations and Demodulation Technique: Continuous Phase FSK (CPFSK)</p>	01	6100.00

	<p>Minimum Shift Keying (MSK) Gaussian Frequency Shift Keying (GFSK) Gaussian Minimum Shift Keying(GMSK) Data rate should be variable and maximum up to 30 Mbps Should be maximum up to 8 array FSK On-board digital data pattern generator as a test pattern Two channel Additive White Gaussian Noise Generator with 10 bits/sample/channel I & Q Channel DACs-10 bit@ Sampling rate 125 MSPS maximum Antialiasing low pass filter with 3dB bandwidth of I & Q channel filter: Sallen Key 6-pole Butterworth with cut-off frequency 13MHz Appropriate nos. of test points with BNC connectors to connect external Oscilloscope or Spectrum Analyzer.</p>		
14.	<p>Training System for study of Wireless Digital communication system This training system should have facility for study of digital communication through wired, wireless. It should cover RF frequency Spectrum analysis, the Un-modulated carrier for Transmission by applying different signals like constant data / sine wave / cosine wave at I channel and Q Channel, the concept of Pulse Shaping to improve Spectral Efficiency. It should also have the study about Digital FIR Filters(RRC Filter. - Interpolation, Decimation [Low Pass Filters]) . Also should be for study & analyze of baseband modulation techniques in time & frequency domain - BPSK, DBPSK, QPSK, DQPSK, OQPSK, p/4-QPSK, /4 DQPSK,8PSK, 8QAM, 16PSK, 16QAM, 16APSK, 32QAM, 32APSK, 64QAM,128QAM,OFDM & Direct Sequence Spread Spectrum System(DSSS),PN codes, types of PN codes, Chip Rate, Spreading Factor, Processing Gain. Specification Maximum Data Rate: 10 Mbps or higher Device Xilinx FPGA Spartan3E XC3S500E Dual 125 MSPS 10-bit D/A converters for I Channel and Q Channel 6-pole Butterworth clock rejection filters Maximum bandwidth: +/- 13 MHz @±0.4dB ripple DAC clock rejection @40 MHz > 84 dBc Output voltage: 1Vpp with 0.85V DC bias JTAG USB connector for FPGA configuration Standard built-in Modulations like BPSK, DBPSK, QPSK, OQPSK, DQPSK, p/4 QPSK, p/4DQPSK, MSK, 8PSK, 8QAM, 16PSK, 16QAM, 16APSK, 32QAM, 32APSK, 64QAM, 128QAM Digital Filters: Interpolation, Decimation and Raised Root Cosine with variable roll-off (a) Internal Data Generator as test pattern External Digital Interface connector for expansion Programmable chip rates up to 10 Mchip/s Spreading codes: - Gold sequences (up to 223 chips) - Maximal length sequences, (max length 223 chips) - Barker codes (length 11, 13) Dual-band (902-928 MHz) or (2.025 - 2.5GHz), quadrature modulator, Low-noise frequency synthesizer can be tuned over entire range by steps of 100, 31.25 or 25 KHz 8 preset frequencies for fast (<2ms) local oscillator frequency tuning Selectable internal / external 10 MHz frequency reference for the frequency synthesizer Gold plated SMA(F) connectors for Base-band and RF Built-in channel impairments generation: AWGN and Frequency Offset (Doppler) Data Acquisition Section: (for both Transmitter & Receiver) - Analog Channel: 2 (CH1 & CH2) - Resolution: 8-bit - Digital Channel: 8 (D0 – D7) - Maximum Real-time Sampling: 100MSPS (Analog + Digital Channel Simultaneously)</p>	01	75000.00

		<ul style="list-style-type: none"> - Memory Depth: 4K - Mode: Y-T (Time-domain View) & X-Y (Constellation View) - Interactive GUI with USB2.0 Interface <p>Maximum output data rate: 10 Mbps Device Xilinx FPGA Spartan3E XC3S500E Dual 10-bit Analog-to-Digital converters, 40 MS/s Selectable internal 40 MHz / external ADC sampling clock (to synchronize multiple receivers)</p> <ul style="list-style-type: none"> - Baseband filtering options: Wideband applications (< 26 MHz) <p>JTAG USB Connector for FPGA configuration Interactive Software with USB 2.0 interface for various Labs Dual-band, [902-928 MHz] and (2.025 – 2.5 GHz) receiver Sensitivity: -56 dBm RF input for full scale 10-bit output samples Built-in RF AGC, 70 dB dynamic range Low phase-noise frequency synthesizer can be tuned over entire range by steps of 100, 31.25, or 25 KHz 8 preset frequencies for fast (<2ms) local oscillator frequency tuning Selectable internal / external 10 MHz frequency reference for the frequency synthesizer SMA connectors Direct Sequence Spread-Spectrum demodulator Variable chip rate up to 10 Mchips/s Spreading codes: <ul style="list-style-type: none"> - Gold sequences (up to 223 chips) - Maximal length sequences, (max length 223 chips) - Barker codes (length 11, 13) BPSK, QPSK selectable Demodulation performances: within 1.5 dB from theory at threshold SNR of 5 dB Sequential code search Receiver lock monitoring using software External Digital Interface connector for expansion Measures actual bit errors while a known PRBS-11 pseudo-random test sequence is being transmitted</p> <p>Equipment for Analyzing the Signals Should be bench top and with All-Digital IF Technology 9 kHz -3.2GHz Frequency Range Frequency Resolution: 1Hz Minimum Resolution Bandwidth (RBW): 10 Hz to 1 MHz, in 1-3-10 sequence Displayed Average Noise Level (DANL): -161dBm Phase Noise: -80dBc/Hz @ 10kHz Offset or better Total Amplitude Uncertainty <1.5dB</p> <p>Triggering Source: Free run, Video, External Impedance: 50 Ω Output Connector: N Type Female Measurement Range: DANL to +20 dBm Connectivity: LAN, USB host, USB device 8 Inch color WVGA (800x480) Display</p>		
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AMC and ESD Lab requirements	1.	PIC controller Kit PIC16F877A MCU clocked at 4 MHz, Expansion connectors for plug in modules and prototyping area, On platform programmer, USB interface to PC for programming, Every pin is marked in order to make work easier, Master Reset/ Restart Key for hardware reset, Input/ output & test points provided on platform, On platform breadboard for connecting external components	10	10000.00
	2.	Interfacing Applications Board, Stepper Control Board, Display &	10	20000.00

		Switch Module, GSM, Application Module		
	3.	Keil kits or ESA MCB 51-2 Evaluation Board	10	10000.00
	4.	ARM9 Development platform Integrated with S3C2440 (16 KB each of instruction and data cache), 4 KB RAM, NAND flash boot loader, power management functions, an interrupt controller and an external memory controller	8	34000.00
	5.	Application for ARM Microcontroller, Stepper Control Board, Display & Switch Module, GSM	10	14000.00

Start Date and Time of uploading of e-tender : 19.12.2019 at 9.00 AM
End Date and Time of uploading of e-tender : 09.01.2020 at 11.00 AM
Date and Time of opening of Online Bid (Technical Bid) : 09.01.2020 at 11.30 AM
Detailed Terms and Conditions are available in e-tender document.

NOTE:-

Note 1:-The tender will be on item-wise basis for each scheme.

Note 2:-The sealed envelope of EMD should bear the Advertisement No., Scheme No./item and should be clearly superscribed as "EMD the purchase of equipments in the Labs of Electronics and Communication Engineering Department due on 09.01.2020 at 11.00 A.M."

NOTE 3. The bidder may note that no column of the BOQ shall be left blank. In case of items for which no bid is being made by the bidder, numeric value 0 (zero) shall be invariably mentioned for the validation of the BOQ.

The bid document can be downloaded from the website of Chandigarh Administration <http://www.etenders.chd.nic.in> . However for general information, guidance and reference, the tenderer can approach to office of Principal, Chd. College of Engg. & Tech. (Degree Wing), Sector-26, Chandigarh (Phone No. 0172-2750943)

Principal

INSTRUCTIONS TO BIDDERS REGARDING E-TENDERING PROCESS

- a. Tenders without Digital Signatures will not be accepted by the electronic tendering system. No tender will be accepted in physical form and in case it has been submitted in physical it shall be rejected.
- b. Before submission of on line bids, bidders must ensure that scanned copies of all the necessary documents have been uploaded with the bid.
- c. Principal, Chandigarh College of Engg. & Technology (Degree Wing), Chandigarh will not be responsible for any delay in online submission of bids due to any reason whatsoever.
- d. Bidders should get ready with the scanned copies of EMD as specified in the tender documents. The original instruments in respect of EMD in the shape of FDR or Deposit at Call or Term Deposit Receipt or Demand Draft in favour of the Principal, Chd. College of Engg. & Tech. (Degree Wing), Sector-26, Chandigarh should reach on or before **09.01.2020 at 11.00 AM.**
- e. The details of EMD specified in the tender document should be same as submitted online (scanned copies). Otherwise tender will be rejected summarily.

TERMS AND CONDITIONS OF THE TENDER

CCET STANDS FOR CHANDIGARH COLLEGE OF ENGINEERING & TECHNOLOGY,

(DEGREE WING), CHANDIGARH.

1. The last date and time for receipt of tenders is **09.01.2020** at **11.00 AM** through e-tendering only.
2. **The Tender will be two Bid Systems i.e. Technical Bid and Financial Bid on Item-wise basis for each scheme.**
 - i) **The Technical Bid will contain technical specifications; and**
 - ii) **The Financial Bid will contain rate per equipment/Item but will be considered on item-wise basis for each scheme.**
 - a) **If rates are quoted along with Technical Bid, it will be rejected straightway.**
 - b) **The Financial Bid(s) of only those firms will be opened who are technically qualified and the date and time for opening of financial bid(s) will be conveyed after opening of the Technical Bid.**
3. After successful completion of Technical qualification, each successful bidder should provide technical demonstration of all equipments. Financial bid should be considered for those bidders which will be recommended by Departmental Purchase Committee after demonstration.
4. Each tender must be accompanied with Earnest Money Deposit for each item as mentioned above in the shape of FDR or Deposit at Call or Term Deposit Receipt or Demand Draft in favour of the Principal, Chandigarh College of Engineering & Technology (Degree Wing), Chandigarh, valid for three months payable at Chandigarh on any Scheduled Bank.
5. The sealed envelope of EMD should bear the Advertisement No., Scheme No./item and should be clearly **super scribed as “EMD for the purchase of equipments in the Labs of Electronics and Communication Engineering Department,** due on **09.01.2020** at **11.00 a.m.** should be separately submitted in the office of Principal, Chandigarh College of Engineering & Technology (Degree Wing), Sector-26, Chandigarh on or before **09.01.2020 upto 11.00 a.m.**
6. Any attempt direct or indirect, to cast influence, negotiation on the part of the tenderer with the officials/authority to whom he will submit the tender or the tender accepting official/authority before the finalisation of tenders will render the tenderer liable for exclusion from consideration.
7. Tender(s) received without earnest money as specified at Sr. No. 3 above shall be rejected straightway.
8. Earnest Money deposited with the Chandigarh College of Engg. & Technology, (Degree Wing), Chandigarh in connection with any other tender will not be considered against this tender.
9. The Public Sector undertaking of the Central / State Govt. are exempted from furnishing Earnest Money Deposit.
10. This tender is not transferable.
11. The tender i.e. Pre-qualifying-cum-Technical Bid shall be opened on **09.01.2020** at **11.30 a.m.** at Chandigarh College of Engineering & Technology (Degree Wing), Chandigarh.
12. Conditional offer shall be rejected.
13. The requirements of the Institute in terms of category of equipments/items/instruments, detailed specifications and quantity are given in **SCHEDULE OF TECHNICAL SPECIFICATION/ REQUIREMENT (AS PER ANNEXURE-I)** for Electronics & Communication Engineering Department. Principal, CCET reserves the right to change the quantity for any/all items without assigning any reason.
14. The tenders not accompanied by Earnest Money or incomplete in any respect will be rejected outrightly.
15. **No advance payment will be made.** Payment will be made after receipt of equipments, its inspection, installation and testing to the satisfaction of the Technical and Technical Purchase Committees.
16. The quoted prices must be mentioned showing GST separately.
17. The Principal, CCET reserves all rights to accept or reject any tender without assigning any reason.
18. **Rates should be quoted F.O.R. Chandigarh College of Engg. & Technology, Sector-26, (Degree Wing) Chandigarh including packaging, forwarding, postage and freight etc.**
19. The Principal, CCET reserves all rights to reject the goods if the same are not found in accordance with the required description / specifications.

20. In case of violation of any term and condition as mentioned, Earnest Money Deposit of the tenderer shall be forfeited in full or part at the entire discretion of the Principal, Chandigarh College of Engg. & Technology, Chandigarh.
21. Training for the operation of equipments, if any, shall be provided by the firm free of cost to the faculty / other staff of the college.
22. The defective equipments/items/ from the Store of Chandigarh College of Engg. & Technology, Chandigarh will be lifted at the entire cost & risk of the firm. Chandigarh College of Engg. & Technology, Chandigarh will not bear any expenses on this account and the instruments lying in the CCET premises will be at tenderer's risk and cost.
23. The equipments/items will be maintained free of charges during the warranty period.
24. **PERFORMANCE SECURITY:-** Performance security @10% of the value of supply order covering the warranty period shall be furnished by the firm in the shape of Bank Guarantee duly pledged in favour of Principal, Chandigarh College of Engg. & Technology, Chandigarh before / along with supply of equipments. **The performance security should remain valid for a period of 60 days beyond the date of completion of all contractual obligations of the supplier including warranty obligations.**
25. The CCET would return the Earnest Money Deposit to the successful tendering firm on the submission of the Bank Guarantee. EMD of unsuccessful tenderer will also be returned.
26. Rates quoted in Indian Currency only shall be accepted irrespective of foreign make of equipments/items which should include all kinds of charges, taxes, duties etc. Financial bids showing the rates in other currency shall not be considered and deemed to be rejected automatically.
27. **PERIOD FOR WHICH THE OFFER WILL REMAIN OPEN:-**
The tendering firms should keep their offers valid for acceptance up to **31-03-2020**. If the firms are unable to keep their offers open for the above said period, they should specifically state the period for which their offers would remain open but such a provision may result in the rejection of their offers.
28. Any conditional tender or any deviation from the terms and conditions of the tender document shall render the tender liable to rejection.
29. The equipments/items will be installed free of charge by the firm / agent at the designated premises. The cost of material required for installation shall be borne by firm. Material for experimental set up such as Table, Stand etc. should be provided by the firm at its own cost. CCET will not provide any material required for installation. Foundations of equipments wherever necessary shall be provided/constructed by the supplier free of cost.
30. **DELIVERY PERIOD:-** The Delivery period of the equipment/items shall be strictly 2-3 weeks from the date of supply order. The delivery period will be extended at the sole discretion of the Principal, CCET in special circumstances on written request from the firm. Penalty @ 1.00% per week of the cost / price of equipment/items for actual period of delay after the due date of supply of equipments/items will be charged.
31. Installation and demonstration will be done by the supplier to the satisfaction of Head of Department concerned.
32. Warranty period, where applicable, should be clearly specified but not less than 1-year in any case.
33. After the receipt of equipments/items, any fault or deficiency in the equipments/items noticed should be rectified by the supplier within two weeks after intimation free of cost.
34. Instructional materials and **e-manuals** will be uploaded by the supplier free of cost.
35. The technical brochure for the equipments shall be uploaded along with Pre-qualifying – cum – Technical Bid.
36. **INSPECTION OF MACHINERY/EQUIPMENT/ITEMS/INSTRUMENTS**
The equipments/items will be inspected only at CCET premises. However, the inspection of equipments/items at factory site or any other place, if any, shall be carried out at the risk and cost of the Tenderer / Bidder. The CCET will not bear any expenses on this account.
37. In the cases of failure or default in the performance or responsibilities or breach of terms and conditions of DNIT or MOU or any agreement of contract between the company / firm / agency / person or any legal entity and CCET, as the case may be, the said company / firm / agency / person or any legal entity shall be black listed in the light of notification issued by Chandigarh Administration vide their letter No. 1927-F&PO(3)-2009/1170 dated 27-02-2009 or any other instructions issued from time to time.

38. **The tenderer has to submit latest affidavit (as per Annexure II) regarding non black listing of individual / firm/ company, as the case may be.**

39. **JURISDICTION**

The courts of Chandigarh alone will have the jurisdiction to try any matter, dispute or reference between the parties arising out of this purchase. It is specifically agreed that no Court outside and other than Chandigarh Court shall have jurisdiction in the matter.

40. **Force majeure:-** Any failure or omission or commission to carry out provision of this tender by tenderer shall not give rise to any claim by one party against the other if such failure or omission or commission arise from an Act of God; which shall include all Acts of natural calamities such as fire, flood, earthquake, hurricane, or any pestilence or from civil strikes, compliance with any status and / or regulation of the Government, lock outs and strikes, riots, curfew, embargoes or from any political or other reason beyond the parties control including war (whether declared or not), civil war or stage of insurrection, provided that notice of the occurrence of any event by either party to the other shall be given within two week from the date of occurrence of such any event which could be attributed to force majeure conditions.

Note 1:-The sealed envelope of EMD should bear the Advertisement No., Scheme No./item and should be clearly superscribed as “EMD the purchase of equipments in the Labs of Electronics and Communication Engineering Department., due on 09.01.2020 at 11:00 A.M.

NOTE 2. The bidder may note that no column of the BOQ shall be left blank. In case of items for which no bid is being made by the bidder, numeric value 0 (zero) shall be invariably mentioned for the validation of the BOQ.

Annexure-I

Schedule of Technical Specification/Requirement

(SPECIFICATIONS AND ALLIED TECHNICAL DETAILS OF EQUIPMENTS/ITEMS AND SCHEDULE OF REQUIREMENT)

Electronics and Communication Engineering Deptt.

(SCHEME NO.._____)

Note 1:- The tender will be on item-wise basis for each Scheme.

Note 2:- The sealed envelope of EMD should bear the Advertisement No., Scheme No. and should be clearly superscribed as “EMD the purchase of equipments in the Labs of Electronics and Communication Engineering Department due on 09.01.2020 at 11:00 A.M.”

NOTE 3:- The bidder may note that no column of the BOQ shall be left blank. In case of items for which no bid is being made by the bidder, numeric value 0 (zero) shall be invariably mentioned for the validation of the BOQ.

ANNEXURE-II

I/We (Name)_____

Contractor / partner / sole proprietor (strike out word which is not applicable) or (Firm)/Company
_____ do hereby solemnly affirm and declare that the individual
firm / companies are not black-listed by the Union or State Government or any autonomous body.

DEPONENT

Address _____

I/We do hereby solemnly affirm and declare that the above declaration is true and correct to the best of my knowledge and beliefs. No part of it is false and nothing has been concealed.

Dated:

DEPONENT

**CHECK LIST DULY FILLED IN TO BE ATTACHED WITH PRE-QUALIFYING-CUM-TECHNICAL
BID FOR THE EQUIPMENT FOR ELECTRONICS & COMMUNICATION ENGINEERING
DEPARTMENT**

- | | | |
|----|--|--------|
| 1. | Whether EMD in the shape of FDR or Deposit at Call or Term Deposit Receipt or Demand Draft valid for three months, for the asked-for amount attached? | Yes/No |
| 2. | Whether tender document duly signed by authorized Signatory attached? | Yes/No |
| 3. | Whether affidavit duly attested by Notary / Executive Magistrate regarding non-black listing of firm Attached? | Yes/No |
| 4. | Whether a list of institutions / organizations where your firm has supplied this item / equipment / instrument recently, is attached. | Yes/No |
| 5. | If you are an authorized agent / dealer / distributor of the firm / company / manufacturer and whether authority letter as issued by them in your favour attached? | Yes/No |
| 6. | Whether Technical broucher of the equipments attached? | Yes/No |

Signature of authorized signatory
with seal of the firm